A NOVEL LOW COST 25μm THIN EXFOLIATED MONOCRYSTALLINE SI SOLAR CELL TECHNOLOGY

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ABSTRACT

To achieve grid parity, photovoltaic (PV) technologies must reduce the production cost of PV modules to well below $1/Wp. In crystalline Si (c-Si) solar cells the cost of raw Si wafers is over 40% of the module cost. There is an industry wide push to reduce the active Si content of the cell through a combination of thinner wafers and increased cell efficiency. However, cell manufacturers are struggling to reduce the wafer thickness below 150μm as there are no economically viable technologies for manufacturing very thin Si wafers and such thin silicon wafers impose stringent handling requirements as wafer breakage and yield loss impact final module cost. In this paper, we demonstrate for the first time, a novel exfoliation technology capable of producing large area (6-in diameter) 25μm thin flexible mono c-Si foils that will dramatically change the cost structure and form factor of high efficiency-Si solar cells without the yield losses and handling issues that are a major problem for traditional thin Si wafers. An un-optimized single side heterojunction cell has been formed with a 25μm exfoliated c-Si foil, which shows an efficiency of 12.5%. The cell characteristics of a 25μm thin c-Si cell with intrinsic a-Si passivation will be presented in the paper. Simulations show that with optimized texturing of the foil and passivation, higher efficiencies (20%) can be attained. Depending on the starting wafer or ingot thickness a final cell cost of between $0.46/Wp to $0.50/Wp can be achieved compared to $1.1/Wp for today's commercial thick crystalline Si cells.

INTRODUCTION

The crystalline silicon (c-Si) photovoltaic industry has continually strived to reduce Si wafer thickness in order to lower cost and improve cell efficiency. However, decreasing wafer thickness below 150μm is challenging due to lack of mature technologies to manufacture such thin wafers and the handling concerns associated with them. The optimum thickness of Si wafers needed for maximizing cell efficiency is the 20-50μm range, provided good surface passivation is achieved [1,2]. In this paper, we demonstrate for the first time, a novel exfoliation technology capable of producing wafer scale 25μm thin flexible mono c-Si foils that can enable high efficiency solar cells at a low cost structure.

CELL FABRICATION PROCESS

We have developed a kerfless exfoliation process [3] to produce 25μm thin exfoliated mono c-Si foils from a parent wafer. Our novel approach involves forming a flexible metal foil over the substrate using an electrochemical deposition process. During this process hydrogen is incorporated from the plating bath into the silicon substrate. Subsequently an annealing process is carried during which internal stresses are created in the substrate due to the thermal expansion mismatch between the metal and the silicon. The incorporation of hydrogen coupled with the thermal mismatch stresses results in exfoliation of a thin c-Si layer from the substrate. The exfoliation is aided with a mechanical wedge, which leads to fracture along a sub-surface plane of the substrate. The thickness of the exfoliated layer is controlled by varying the electroplated metal thickness, the annealing, and the mechanical wedge parameters. Figure 1 shows a picture of 5-inch diameter exfoliated 25μm thin flexible c-Si foil and its residual parent wafer. Up to 6X repeated exfoliations from a 500 μm thick parent wafer have been demonstrated in our laboratory

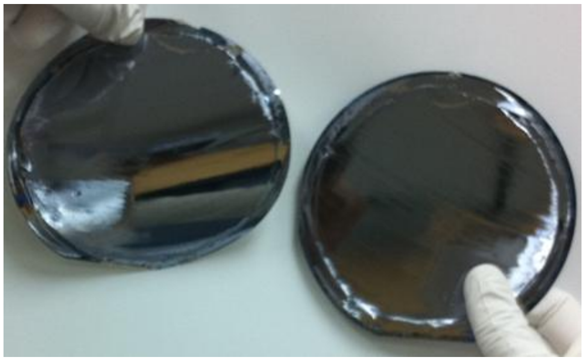

Figure 1. Picture of 5-inch diameter 25μm thin Si foil along with the residual wafer after exfoliation

We have fabricated single heterojunction solar cells using the 25μm c-Si foils that were exfoliated from 500 μm thick (100) and (111) monocrystalline CZ 1-10 ohm-cm low lifetime (< 100μs) Si wafers. As shown in figure 2, the cell fabrication process begins with forming a diffused n+ c-Si junction on the starting wafer using a $POCl_3$ furnace process or spray diffusion process. The next step involves forming a passivation layer over the doped surface using a dielectric such as thermal SiO_2 or hydrogenated-SiN_x. This passivation film is then patterned to open up contact holes and a thick metal film is electrochemically deposited over the Si substrate. Subsequently a 25μm thin c-Si foil is exfoliated from the wafer using the process previously described. Then an amorphous-Si heterojunction is deposited using PECVD over the exfoliated surface. This is followed by ITO sputter deposition. Finally silver grid

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lines are formed by a screen printing and firing process using a low temperature silver paste.

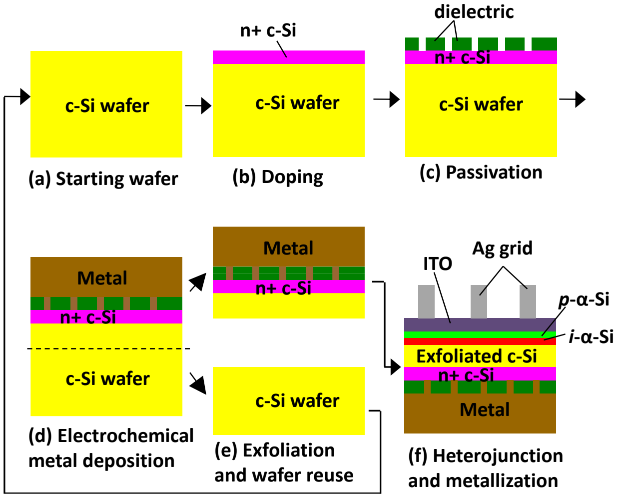


Figure 2. Process flow for fabricating exfoliated single heterojunction solar cells

RESULTS

The process of exfoliation does not degrade the material quality of the foil or the parent wafer. Figure 3 shows a high resolution TEM cross section of a typical exfoliated foil. The lattice fringes observed in the TEM image indicate good crystallinity of the foil after the exfoliation process and absence of dislocations or defects. The good crystallinity of the exfoliated foil helps in preserving the bulk minority carrier lifetime of the starting wafer. Lifetime measurements of the parent wafer before and after exfoliation have shown almost no degradation in minority carrier lifetime (~ 350µs). Furthermore, simulations indicate that as the cell thickness decreases to 25µm, the sensitivity to minority carrier lifetime decreases significantly and a 20% efficient cell can be fabricated even if the lifetime of the foil is only 16µs provided good passivation of both surfaces (SRV < 100cm/s) is achieved [4].

Figure 4 shows the I-V curve from a 9.1mm x 9.1mm area of the cell. The cell characteristics are shown in the table below the figure. The typical efficiency of our unoptimized devices (without intrinsic a-Si passivation and texturing) is 12% with a highest efficiency of 12.5%. The V_{oc} is lower than typical heterojunction cells because of the absence of both the intrinsic a-Si on the front side and a high quality SiNx / oxide passivation on the backside. Furthermore, the backside metal contact area fraction is almost 25% in these samples. As the metal contact fraction is reduced to 5% and lower the V_{oc} is expected to increase as potential recombination sites are minimized. The high current density of the foil indicates that there is some degree of internal light reflection in the exfoliated foil due to the metal and dielectric on the backside. It is expected that the current will improve further with texturing. We have demonstrated texturing of the exfoliated foil on test samples, but not yet implemented in the final cell. Texturing the front surface of the foil in combination with the metal/dielectric reflector at the back is expected to lead to multiple passes of light through the exfoliated foil.

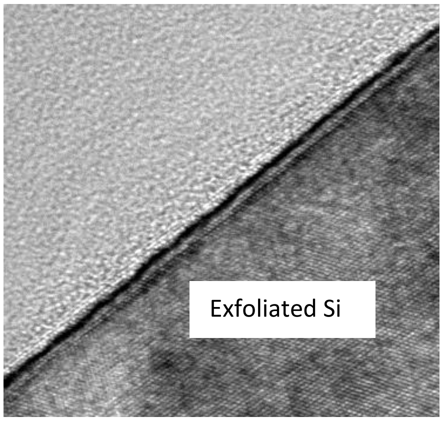
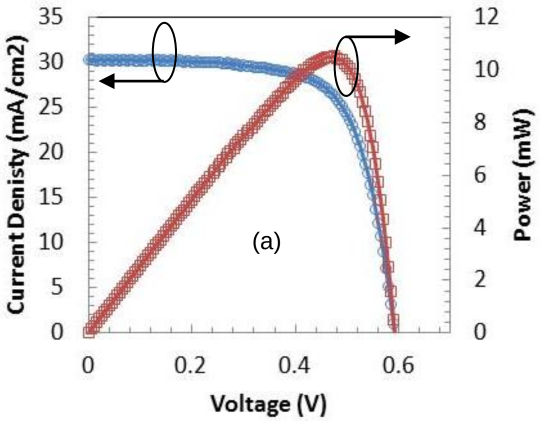


Figure 3. HRTEM image of exfoliated Si foil showing lattice fringes. No defects or dislocations are seen.



V_{oc}	590mV
J_{sc}	30.26 mA/cm^2
Fill Factor	70%
Efficiency	12.5%

Figure 4. I-V characteristic of a 9.1mm x 9.1mm solar cell formed on a 25µm thin exfoliated c-Si foil.

Figure 5 shows the suns-V_{oc} curve from a foil before ITO metallization. The measured V_{oc} is marginally higher than the measured I-V curve indicating that the ITO and metallization need to be optimized in our cell. The slope of the suns-V_{oc} curve indicates that the shunt resistance of the exfoliated cell is high implying that there are no pinholes in the exfoliated Si. Furthermore, the Ag metal grid was formed with a manual hand held screen printer using 9mm x 9mm test patterns, which leads to 28% front grid shading on our cells. It is expected that with optimized screen printing and reduced shading the cell characteristics will further improve.

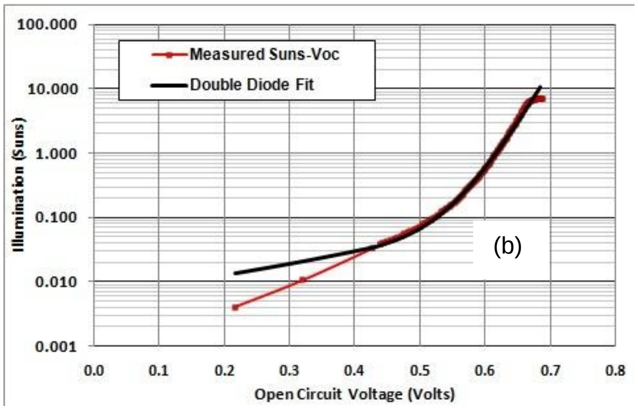


Figure 5. Suns-V_{oc} curve of a foil before metallization.

The low V_{oc} observed for the sample in Fig 4 suggests that the passivation quality is not yet optimized on our cells. Back-surface recombination can be reduced by reducing the back metal contact area and passivating most of the back surface with thermal oxide, and Auger recombination in the back surface field (BSF) region can be reduced by introducing local BSF, which we plan to incorporate in our optimum device.

To get physical insights about local BSF and back side metal contact design we set up FLOODS for reliable physics-based numerical simulation in AM1 (92.5mW/cm^2) sunlight [2]. Modeling of optical carrier generation rate, recombination rates (SRH and band-to-band Auger), mobility, energy-bandgap narrowing and F-D statistics in heavily doped regions is done. An n-type base (N_b ~ 10^{16}/cm^3) is used in our simulation; similar results for p-starting wafers can be projected from the simulations discussed here. In this study, to analyze the effects of the backside metal contact area, doping and passivation, we have assumed the front surface to be an ideal diffused shallow p+-n junction with a uniform top contact and front SRV of 1cm/s.

The local BSF structure eliminates auger recombination near the back of the cell potentially improving Voc. However, the absence of uniform BSF puts a stringent requirement on the back surface passivation. Further, since the local BSF width is small compared to the device width, a heavy doping profile is required to achieve sufficient built-in electric field. For our FLOODS simulation, we assume ohmic back contact (with surface recombination velocity S=10^6cm/s), base doping density $N_B=10^{16}$/cm^3, minority hole lifetime of τ_p ~ 1ms and local BSF with Gaussian profile and surface doping density N_S=3E20/cm^3, junction depth xj=0.3µm and metal contact width w_m=2µm.

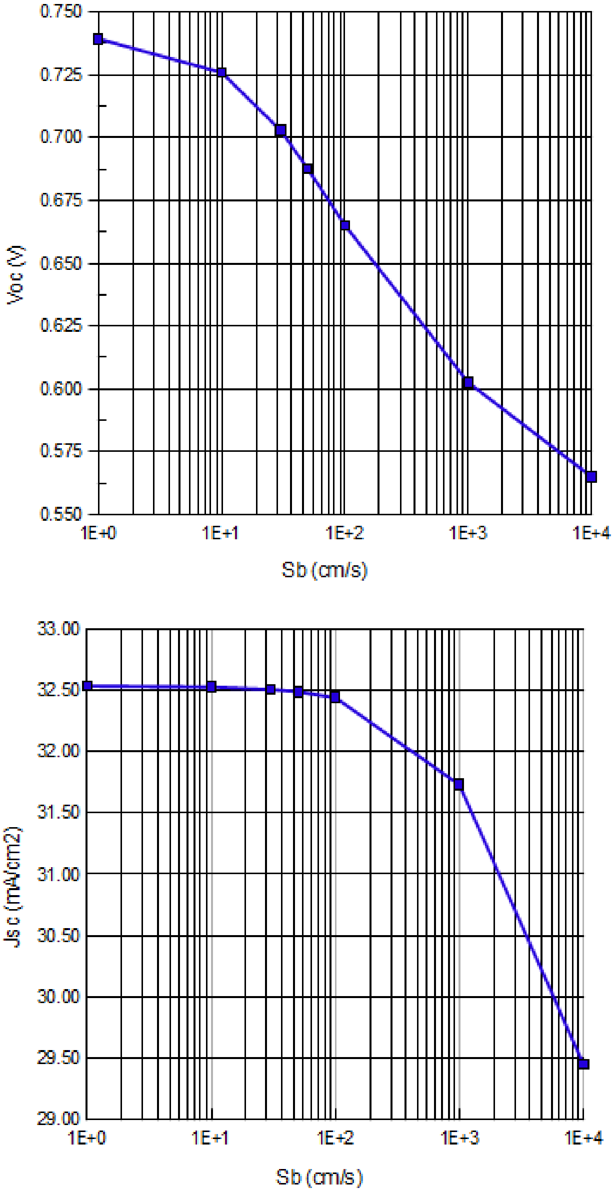


Figure 6. FLOODS-predicted V_{oc} and J_{sc} dependence on back surface passivation with contact width wm=2µm and pitch of 300µm under AM1 (92.5mW/cm2) spectrum. For a S_b of ~50cm/sec, V_{oc} ~ 0.68 and J_{sc} of ~ 32.5mA/cm2 are attained without any internal light reflection

Figure 6 shows the high V_{oc} and J_{sc} achievable with such a local BSF design. The V_{oc} decreases for S_b > 30cm/s due to recombination at the non-metal back surface and for S_b > 100cm/s the J_{sc} also decreases. For longer minority carrier lifetime, the V_{oc} is directly impacted by the non-metal back surface recombination. However, J_{sc} is comparatively less affected by S_b because most of the electron-hole pairs generated by photon absorption are at the top of the device that are collected efficiently by front junction and the built-in electric field emanating from n+ region helps drive minority holes away from back surface when S_b is small.

SIGNIFICANCE AND CONCLUSIONS

With this novel process, we are able to address the three key challenges in the technology roadmap for c-Si solar cells – efficiency, cost and form factor. The metal backing of our exfoliated foils, in combination with our back junction architecture, provides internal light reflection that is needed for such thin c-Si cells to increase the generation current. Furthermore, the metal backing of the foil lends it flexibility making it easier to handle compared to other thin c-Si approaches, which produce fragile wafers. Our novel process ensures that there is no handling of thin Si in the line and also enables multiple exfoliations and starting wafer reuse. The savings in Si wafer costs translate into a final cell cost of less than $0.50/Wp compared to ~ $1/Wp for thick crystalline Si screen printed cells.

In summary, we have demonstrated an exfoliation technology that provides a disruptive solution with the potential for low cost high volume production of wafer scale thin 25µm Si foils and enable high efficiency solar cells. A 12.5% efficient solar cell has been fabricated using an unoptimized single heterojunction cell process to demonstrate the potential of this technology. Simulations show that with optimized cell fabrication processes higher efficiencies of ~ 20% can be attained.

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